Tuning Resistive Switching Characteristics of Tantalum Oxide Memristors through Si Doping

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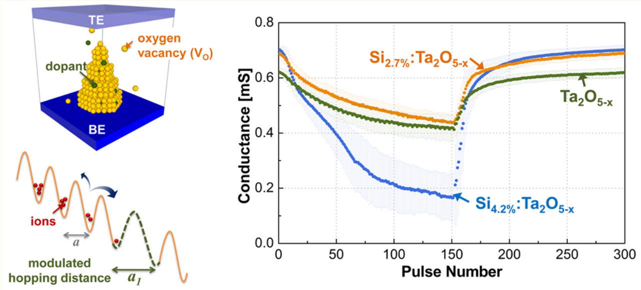

ABSTRACT An oxide memristor device changes its internal state according to the history of the applied voltage and current. The principle of resistive switching (RS) is based on ion transport (*e.g.*, oxygen vacancy redistribution). To date, devices with bi-, triple-, or even quadruple-layered structures have been studied to achieve the desired switching behavior through device structure optimization. In contrast, the device performance can also be tuned through fundamental atomic-level design of the switching materials, which can directly affect the dynamic transport of ions and lead to optimized switching characteristics. Here, we show that doping tantalum oxide memristors with silicon atoms can facilitate oxygen vacancy formation and transport in the switching layer with adjustable ion hopping distance and drift velocity. The devices show larger dynamic ranges with easier access to the intermediate states while maintaining the extremely high cycling endurance (>10^{10} set and reset) and are well-suited for neuromorphic computing applications. As an example, we demonstrate different flavors of spike-timing-dependent plasticity in this memristor system. We further provide a characterization methodology to quantitatively estimate the effective hopping distance of the oxygen vacancies. The experimental results are confirmed through detailed *ab initio* calculations which reveal the roles of dopants and provide design methodology for further optimization of the RS behavior.

KEYWORDS: memristor · dopant · hopping · oxygen vacancy · tantalum oxide · resistive switching

Memristors and memristive systems have attracted tremendous attention as possible candidates for future memory and logic applications.[1−5] By tuning an (or a set of) internal state variable(s), a memristor can show either abrupt (*i.e.*, digital) or incremental (*i.e.*, analog) change in resistance. The inherent memory effect in these simple two-terminal devices allows efficient data storage and programmable signal routing. In particular, computing systems based on non-von Neumann architectures, such as neuromorphic systems, have been studied extensively where spike-driven synaptic plasticity in neural synapses can be emulated using the analog resistive switching (RS) behavior of memristors.[6−8]

In widely studied oxide-based memristors, the RS behavior is believed to be caused by the transport of oxygen ions (O^{2-}) and consequent oxygen vacancy (V_O) redistribution in the oxide layer, where high V_O concentration regions (*e.g.*, conducting filaments (CFs)) provide high conductance channels for electrical transport.[9] The device can be set (from a high resistance state (HRS) to a low resistance state (LRS)) or reset (from LRS to HRS) between the different resistance states according to the formation/rupture of the CFs. Although a single oxide layer can attain this RS behavior in memristors,[1,5,10] bi-,[11,12] triple-,[13] or even quadruple-layered[14] oxides have been explored in recent years to improve the switching characteristics. The additional oxide layers act as O^{2-} or V_O reservoirs and can improve the device reliability (*e.g.*, cycling endurance or switching uniformity) by confining RS at selected layers.[11,12] In other cases, the additional oxide layer serves as a tunneling barrier, which induces current nonlinearity by suppressing the leakage current at the low-voltage regime.[13] However, although these extra layers improve the RS controllability, device-to-device variations

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and fabrication complexity increase as the number of oxide layers increases, potentially affecting high-density device integration. Therefore, providing a fundamental atomic-level design that can directly control the dynamic transport of ions within the switching layer not only allows tuning of the RS behavior but also significantly expands the parameter space for material and device optimization, which will be critical for continued development of memristor devices.

In this paper, we show that the RS dynamics in a tantalum-oxide-based bilayer memristor can be modulated through doping of Si atoms in the Ta_2O_{5-x} switching layer. The additional dopant modifies the atomic structure and creates preferred V_O transport channels. Even a small amount of dopants can significantly affect the V_O drift process and change the ion hopping distance and drift velocity, thus allowing control of the RS process at the atomic level. The roles of the dopants were revealed through *ab initio* calculations and confirmed experimentally by extracting the effective V_O hopping distance through a series of measurements. Finally, we show the Si-doped tantalum oxide bilayer memristor devices can emulate different synaptic plasticity with excellent cycling endurance and are suitable for future neuromorphic computing applications.

RESULTS AND DISCUSSION

Improving the RS characteristics through doping by metallic impurities has been attempted recently in HfO_2-based[15,16] or ZrO_2-based[17] devices aimed to improve memory performance. These previous studies show that improved RS behavior, particularly LRS and HRS distribution, can be obtained through doping by providing a better controlled RS path. In this study, we show that doping of the technically important tantalum oxide device with a common element, Si, can improve the dynamic range and provide accessible intermediate states during the RS, while maintaining the extremely high endurance properties of tantalum oxide devices, thus making these devices ideally suited for neuromorphic applications as well. Additionally, quantitative analysis of the V_O drift processes was carried out through a carefully designed experimental procedure and verified through detailed *ab initio* calculations that reveal the role of Si doping on V_O transport.

Figure 1a shows a conceptual schematic to explain the RS behavior in an oxide memristor. The CF corresponds to the region with agglomerated V_O, which controls the local electrical and thermal conductance properties.[9,18] The set and reset processes are described by the ionic transport and consequent V_O migration processes induced by the local electric field and temperature due to Joule heating. The nonlinear ionic transport under high electric field can be explained by the simple rigid-point-ion model shown in Figure 1b.[19−21] Oxygen ions (equivalently V_O) hop among the energy potential wells (assumed to have hopping distance a and energy barrier E_a), where the applied electric field E lowers the energy barriers by a factor of qaE. The average V_O drift velocity is given as

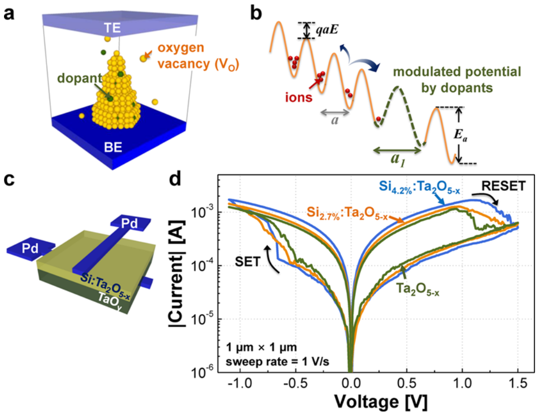


Figure 1. (a) Conceptual schematic of the oxide memristor during RS. The agglomerated oxygen vacancies enhance the local electrical conductivity and form the CF. (b) Schematic of the potential energy landscape for ion hopping under electric field *E*. (c) Schematic plot of the Pd/Si:Ta_2O_{5-x}/TaO_y/Pd bilayer memristor device. (d) Direct current *I*−*V* characteristics of undoped Ta_2O_{5-x}, $Si_{2.7\%}$:Ta_2O_{5-x}, and $Si_{4.2\%}$:Ta_2O_{5-x} devices. The measured device size is 1 μm × 1 μm, and the voltage sweep speed is 1 V/s.

$$v = a \cdot f \cdot \exp(-E_a/kT) \cdot \sinh(qaE/2kT) \qquad (1)$$

where f, k, T, and q are the frequency of escape attempts, Boltzmann constant, temperature, and electron charge, respectively.[9,21] From this equation, one can see that the V_O drift is a strongly nonlinear function of the applied electric field E through the sinh function, where the effect can also be strongly affected by the hopping distance a, which can in turn be affected by doping, as schematically shown in Figure 1b. In other words, the RS behavior controlled by the ion hopping process can be fundamentally optimized at the atomic level through doping. To demonstrate this concept, a tantalum-oxide-based bilayer memristor with Si dopants was fabricated, which consisted of a resistive, Si-doped Ta_2O_{5-x} film as the RS layer and a conductive TaO_y film as the V_O reservoir (see Methods and Supporting Information).[11,13] These two layers were sandwiched by top and bottom Pd electrodes (TE and BE), as shown in Figure 1c. The Si dopants were introduced by a co-sputtering process during the Ta_2O_{5-x} film deposition where the atomic percentage of Si was controlled by the sputtering power, as confirmed by X-ray photoemission spectroscopy (XPS; see Figure S1).

Figure 1d shows dc *I*−*V* characteristics in three different devices based on RS layers of undoped Ta_2O_{5-x}, $Si_{2.7\%}$:Ta_2O_{5-x}, and $Si_{4.2\%}$:Ta_2O_{5-x}, respectively, during the set and reset processes. Noticeable differences can be found when Si dopant is added: (1) the current level at the LRS increases; (2) the current level at the HRS decreases; and (3) the set voltage (defined as the

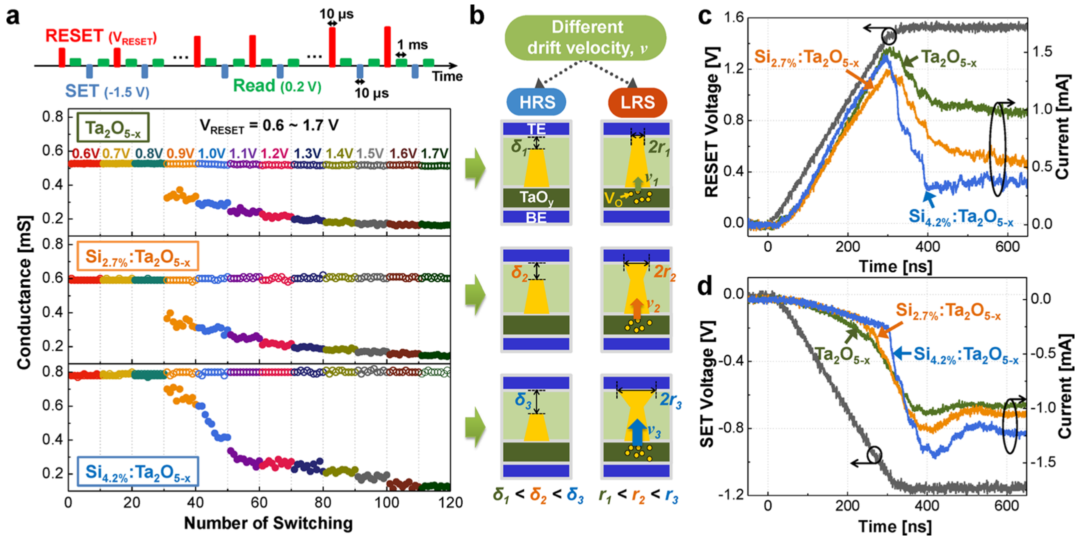


Figure 2. (a) Switching dynamics characterized by pulse measurements with increasing reset-pulse amplitudes. The set-pulse amplitude is fixed at −1.5 V. Before the pulse measurements, the devices are set to LRS with a dc voltage sweep. (b) Schematic of the HRS and LRS for different V_O drift velocities. δ and r increase as v is increased through Si doping. (c) Time-dependent switching transient during the reset and (d) set processes.

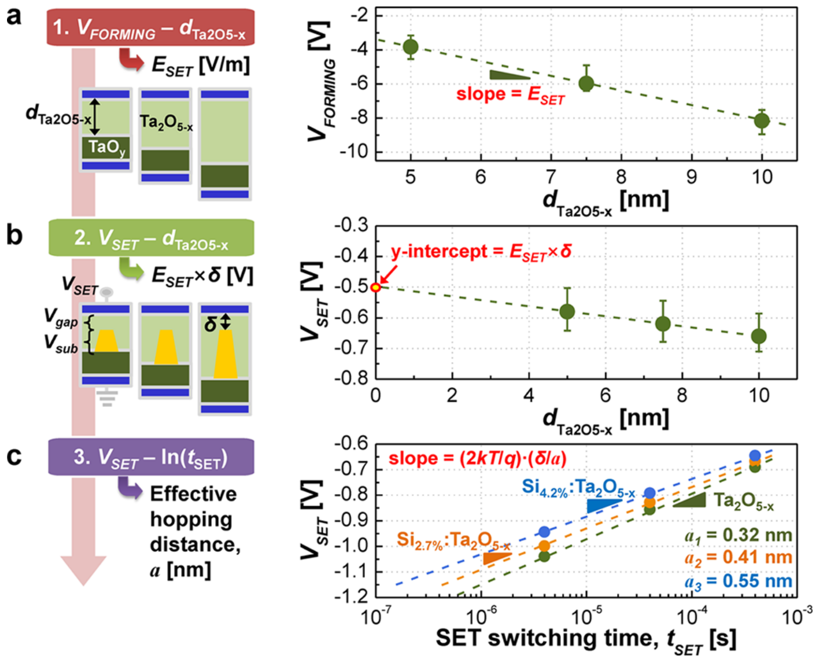
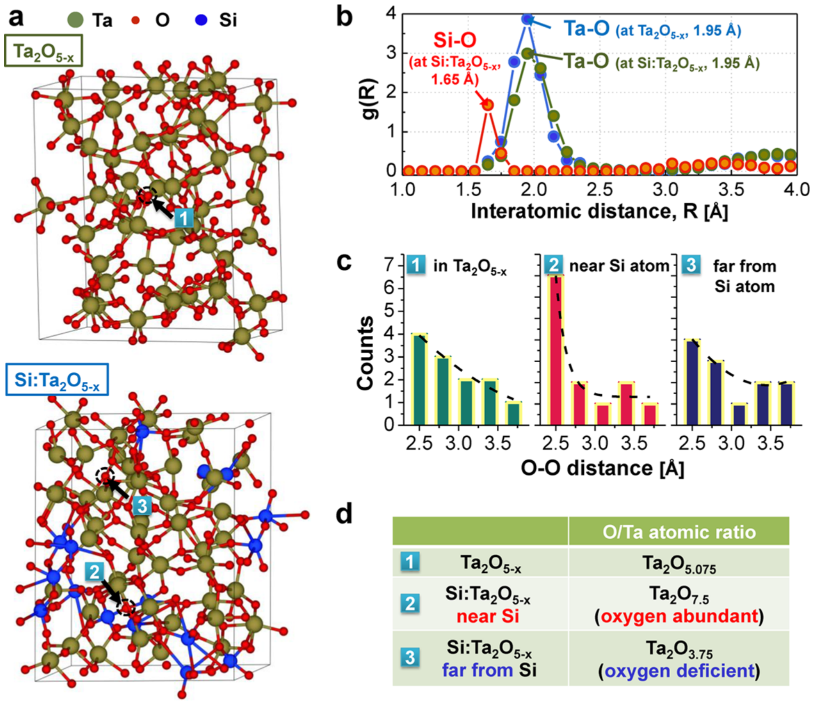


Figure 3. Three-step measurement procedure to evaluate the effective hopping distance. (a) $V_{FORMING}-d_{oxide}$ plot to evaluate E_{SET}; the slope represents E_{SET}. (b) $V_{SET}-d_{oxide}$ plot to estimate δ; the y-intercept represents $E_{SET}\cdot\delta$. (c) $V_{SET}-\ln(t_{SET})$ plot to extract a; the slope represents $(2kT/q)\cdot(\delta/a)$.

voltage when the current begins to increase abruptly) increases. These different switching behaviors indicate that the formation/rupture of the CFs is modulated by the Si dopant. These effects are observed more clearly in pulse switching tests. Figure 2a shows the evolution of the device conductance as a function of the reset-pulse amplitude, by keeping the set-pulse amplitude constant while increasing the reset-pulse amplitude from 0.6 to 1.7 V during repeated set and reset processes. A more conductive LRS and a more resistive HRS are clearly obtained in the Si-doped devices. In a generally accepted theory,[22] the difference in HRS and LRS can be explained by the evolution of the CF shape during switching: a thicker CF radius (r) inside the switching layer leads to higher current at the LRS (*i.e.*, more conductive LRS), and a wider depleted gap length (δ) between the TE and CF tip leads to lower current at the HRS (*i.e.*, more resistive HRS), as shown in Figure 2b. These results thus suggest that Si doping allows the V_O to drift faster under the electric field during set/reset that leads to lower LRS resistance and higher HRS resistance. The V_O drift will also be



		O/Ta atomic ratio
1	Ta_2O_{5-x}	$Ta_2O_{5.075}$
2	$Si:Ta_2O_{5-x}$ near Si	$Ta_2O_{7.5}$ (oxygen abundant)
3	$Si:Ta_2O_{5-x}$ far from Si	$Ta_2O_{3.75}$ (oxygen deficient)

Figure 4. (a) Snapshots of the amorphous Ta_2O_{5-x} and Si-doped Ta_2O_{5-x} structures obtained in the *ab initio* simulation. The Ta, O, and Si atoms are colored in dark green, red, and blue, respectively. (b) Pair-correlation functions of the amorphous Ta_2O_{5-x} and Si-doped Ta_2O_{5-x} calculated at room temperature. (c) Histograms of the O−O distance from a selected oxygen atom to a neighboring oxygen atom. Three oxygen atoms are selected randomly, as shown in panel a. (d) O and Ta atomic ratio near the selected oxygen atoms.

accelerated by Joule heating effects.[9,18,19] For example, during the set process, a fast V_O drift (field-driven) leads to a fast decrease of device resistance, which results in enhanced Joule heating accelerating the V_O drift further.[9,18,19] During reset, the lower LRS may also cause higher Joule heating and lead to a faster V_O drift[9,18,19] (thermally accelerated) and, consequently, a wider depleted gap. To accurately observe the time-dependent drift process, the transient response of the RS was measured, as shown in Figure 2c,d (see Method). We observed that the Si-doped devices show faster resistance transitions during set and reset processes, which again indicates a faster V_O drift process. Therefore, the different RS behaviors *via* Si doping can be understood by the faster V_O drift process: during set, the V_O can be easily supplied from the TaO_y layer under the same applied electric field, leading to larger CF formation and a more conductive LRS, while during reset, the V_O can be more easily depleted, leading to a wider gap δ and a more resistive HRS, as shown in Figures 3b and S6b.

As shown in eq 1, the difference in V_O drift velocity can be explained by the modulation of the hopping distance *a*. To estimate the effective hopping distance in the switching layer, we developed a method on the basis of a series of simple electrical measurements. Figure 3 shows a three-step measurement procedure to evaluate the effective hopping distance. First, Figure 3a shows the measured forming voltage ($V_{FORMING}$) according to different switching layer thicknesses (d_{oxide}) to evaluate the critical electric field (E_{SET}) that initiates V_O migration. (Data of the Si-doped layers are shown in Figures S3 and S4 in the Supporting Information.) We assume that the entire forming voltage is applied on the switching layer, and the voltage drops in the much more conductive electrodes and the TaO_y layer are neglected. Then, E_{SET} can be estimated from the slope of the $V_{FORMING}-d_{oxide}$ plot on the basis of the relationship $V_{FORMING} = E_{SET} \times d_{oxide}$. Second, V_{SET} as a function of different d_{oxide} values is measured to evaluate δ of the CF. When the set process is initiated by V_{SET}, the applied V_{SET} is divided into two parts, as shown in Figure 3b, that is, $V_{SET} = V_{gap} + V_{sub}$. V_{gap} is applied across the gap δ and can be expressed as $V_{gap} = E_{SET} \times \delta$. We assumed that δ is mainly determined by the reset conditions and will be constant at a given reset condition regardless of d_{oxide}. On the other hand, because the length of the remnant CF (hence its resistance) is proportionally increased with the increase of d_{oxide}, V_{sub} is to first-order proportional to d_{oxide}. Thus, V_{gap} ($=E_{SET} \cdot \delta$) can be extracted from the *y*-intercept value of the $V_{SET}-d_{oxide}$ curve; consequently, δ is estimated using the evaluated E_{SET} in the first measurement. The experimentally extracted δ is consistent with the estimated values by previous studies,[18,23] and δ increases from 0.58 to 0.71 nm with the addition of the Si dopant as shown in Figure S6b at the same set and reset conditions, consistent with the observed more resistive HRS behavior in the Si-doped devices shown in Figure 2a. Finally, the effective hopping distance can be estimated from the slope of the V_{SET}−ln(t_{SET}) curve, where t_{SET} is defined when the normalized conductance change ratio reaches two and the slope is expressed as $(2kT/q)\cdot(\delta/a)$ (the model details are explained in the Supporting Information). From these three-step measurements, the effective hopping distance can be quantitatively extracted, where a increases from 0.32 to 0.55 nm as the Si dopant is added, which contributes to a faster drift process, as predicted in eq 1, and explains the experimentally observed higher HRS and lower LRS in Si-doped devices shown in Figures 2c,d.

A question remained as to why the effective hopping distance is increased by the Si dopant. It has been believed that the hopping distance corresponds to the spacing between oxygen sites in the oxide.[24] To understand the nature of the hopping distance (and oxygen sites) modulation by dopant, we performed first-principle electronic structure calculations on the basis of the density functional theory using the Vienna ab initio simulation package (VASP). Figure 4a shows the calculated atomic structure of both undoped Ta_2O_{5-x} and Si-doped Ta_2O_{5-x} where a quenched amorphous Ta_2O_{5-x} structure was used to better represent the experimental system, which is in contrast to previous *ab initio* studies based on crystal structures[15−17] (the detailed methods to generate the atomic structure are described in the Supporting Information). Figure 4b shows the calculated pair correlation function, which represents the probability of finding the center of a particle a given distance away from the center of another particle. In the undoped Ta_2O_{5-x} case, the interatomic distance between Ta and O is 1.95 Å. When Si dopant is added, this Ta−O interatomic distance does not change. However, the interatomic Si−O distance is found to be shorter than the Ta−O distance, implying that oxygen can be located closer to Si than to Ta. In addition, the interatomic distances among oxygen atoms are investigated. Figure 4c shows the calculated O−O distance from the selected oxygen atom to a neighboring oxygen atom. We select three arbitrary oxygen atoms, as shown in Figure 4a: (1) an oxygen atom located in undoped Ta_2O_{5-x} (case 1), (2) an oxygen atom located near a Si atom in $Si{:}Ta_2O_{5-x}$ (case 2), and (3) an oxygen atom located far away from the Si atoms in $Si{:}Ta_2O_{5-x}$ (case 3). The calculated O−O distance in Ta_2O_{5-x} is centered around 0.3 nm, which is consistent with the measured hopping distance (0.32 nm, shown in Figure 3c). In addition, the O−O distance near Si (case 2) appears to be shorter than those of the other cases. From the data shown in Figure 4b,c, we can conclude that the Si dopant more strongly attracts oxygen than Ta, and the oxygen atoms near Si are closely gathered. As a result, the region away from the Si dopant will turn into an oxygen-deficient state. This is confirmed by the *ab initio* calculations in Figure 4d, which plots the calculated O and Ta atomic ratio in the three cases and indicates that an oxygen-deficient region is formed away from the Si dopant. The oxygen-deficient regions facilitate V_O transport in the Si-doped devices as the V_O can hop interstitially (*i.e.*, oxygen-deficient region away from Si dopant) or by substitution through the closely gathered oxygen atoms (*i.e.*, oxygen-abundant region near Si dopant), as shown in Figure S7. These processes allow effective ion hopping and explain the faster V_O drift under electric field in Si-doped devices.

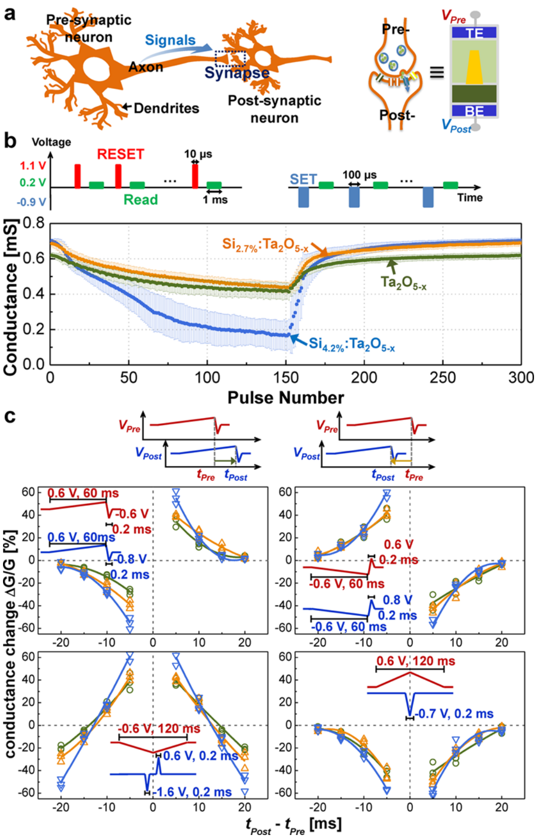


Figure 5. (a) Schematic illustration showing a synapse connecting a pair of neurons, where the synaptic functions can be emulated by memristors. (b) Analog switching behavior obtained by pulse trains consisting of 150 reset pulses (1.1 V, 10 μs) followed by 150 set pulses (−0.9 V, 100 μs) with small, nonperturbative read voltage pulses (0.2 V, 1 ms) applied in the intervals. The conductance changes are measured during the read pulse and plotted as a function of applied pulse number. The error bars indicate the standard deviation from the measured data set, which are collected from 50 such test cycles in five different devices in each case. (c) Implementing four different types of STDP using tantalum oxide memristor. The prespike voltage (V_{Pre}) and postspike voltage (V_{Post}) are applied to the TE and BE of the memristor, respectively. The net programming voltage ($V_{Pre} - V_{Post}$) applied across the device depends on the positive or negative moments $t_{Post} - t_{Pre}$. The dots indicate the experimental data, and the lines are guides for the eye. The insets show the (red) pre- and (blue) postsynaptic spike schemes.

Tantalum oxide memristors have been extensively studied due to its excellent endurance of over 10^{12}, which is the largest among all reported memristive devices.[11] However, the previously reported devices

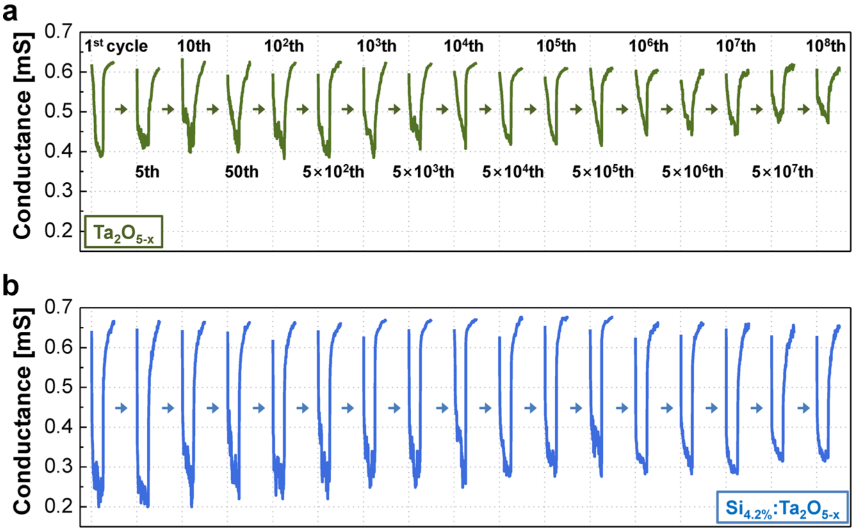


Figure 6. Measured cycling endurance performance of analog switching in (a) Ta_2O_{5-x} memristor and (b) $Si_{4.2\%}$:Ta_2O_{5-x} memristor. Each test cycle consists of a pulse train including 50 reset (1.25 V, 10 μs) pulses followed by 50 set (−1.0 V, 10 μs) pulses.

show mostly digital switching with limited dynamic range. Si doping improves the RS tunability and also makes intermediate states more accessible, making these devices also suitable for neuromorphic applications. In a neuromorphic system based on memristors, the memristor, whose weight can be incrementally modulated by electrical pulses ("spikes"), acts as a synapse connecting a pair neurons, as shown in Figure 5a.[25] Figure 5b shows the measured conductance values in the aforementioned three different samples during the application of pulse (spike) trains. Each pulse train consists of 150 reset (depression) or set (potentiation) pulses, followed by read voltage pulses in the intervals. More intermediate states between maximum and minimum conductance in both the set and reset responses are clearly observed in the Si-doped devices as the number of applied pulses increases, offering a much larger dynamic range compared to the undoped devices. Further increasing the Si doping level results in higher dynamic range, but the switching becomes more digital-like due to the large hopping distance[18] (see Supporting Information, Figure S8).

Here, the more conductive LRS and consequently larger reset current in the Si-doped device may lead to higher power consumption during reset. However, this problem can be mitigated since Si doing also causes more resistive HRS and a larger dynamic range. As shown in Figure 5b, although the maximum LRS conductance of the Si-doped device is higher than that of the undoped device, many intermediate conductance states with values lower than that of the undoped device can be obtained. The overall power consumption can be reduced if the devices are mostly cycled between these states, for example, as analog switches in neuromorphic applications. In addition, the conductance variation of the Si-doped devices appears larger than the undoped devices. We hypothesize that this larger variation may be caused by the larger hopping distances due to Si doping. With larger hopping distance, the stochastic properties of ion hopping will be more pronounced since the stochastic movement of just a few ions may already cause significant resistance changes which in turn affect the dynamic CF growth and dissolution processes, causing variations in the CF shape and resistance variations.[26−28] On the contrary, small hopping distances mean many ions need to be moved to cause significant resistance change so the stochastic hopping properties of individual ions are more effectively averaged out, leading to smaller conductance variations.

The ability of the Si-doped tantalum oxide devices was further tested by implementing spike-timing-dependent plasticity (STDP) learning rules.[6,8] STDP refers to the effect that the relative timing of pre- and postsynaptic spikes determines the sign and magnitude of the long-term synaptic weight change, which can potentially appear in four different forms.[29−31] These four different STDP forms are successfully implemented in our tantalum-oxide-based memristors by designing spike-pairing protocols, as shown in Figure 5c. Clearly, the extent of conductance change depends on the amount of Si dopant, and improved analog performance is obtained through Si-doped tantalum memristors.

Finally, we show that the excellent cycling property of the tantalum oxide memristors is preserved after Si doping, as shown in Figure 6. The 4.2% Si-doped device still maintains analog RS behavior over 10^8 test cycles, with each test cycle containing 50 reset and 50 set pulses corresponding to over 10^{10} total set/reset operations. This reliable analog RS behavior ensures stable long-term operation and will help the development of large-scale memristor-based neuromorphic systems with designable synaptic functions.

CONCLUSION

In conclusion, we show that the RS behavior in memristors can be systematically tuned at the atomic level through doping. Specifically, Si doping can cause faster V_O drift and improves the RS characteristics and leads to more controllable analog switching behavior. A measurement methodology was developed to extract the hopping distance and the depleted gap length during V_O migration. The experimental findings were supported by *ab initio* calculations. We believe these results not only produce a desired memristor system that can be directly used in neuromorphic computing applications but also provide guidance for continued design and optimization of this important class of devices.

METHODS

Device Fabrication. The memristor devices used in this work with a size of 1 μm × 1 μm were fabricated in a crossbar structure on SiO_2 (100 nm)/Si substrates with electrodes patterned using traditional photolithography (GCA AS200 AutoStep). First, a 35 nm bottom Pd electrode was deposited by photolithography, e-beam evaporation, and lift-off processes. Next, a 30 nm TaO_y base layer was deposited by dc reactive sputtering of a Ta metal target in an Ar/O_2 gas mixture at 400 °C. The total pressure of Ar/O_2 was ~5 mTorr, and the oxygen partial pressure in the Ar/O_2 mixture was 3%. A 5 nm Ta_2O_{5-x} switching layer was then deposited by RF sputtering using a Ta_2O_5 ceramic target, and p-doped Si was co-deposited with Ta_2O_{5-x} by dc sputtering (dc power was 40, 70, and 140 W to achieve effectively 2.7, 4.2, and 9.3% Si doping, respectively) in Ar with a pressure of ~5 mTorr. A 30 nm top Pd electrode was then deposited by photolithography, e-beam evaporation, and lift-off processes. Finally, a reactive ion etching process using SF_6/Ar was performed to expose the bottom contacts. For the forming step, a resistor (5 kΩ) was serially connected to the device to prevent permanent breakdown.

Alternating Current Transient Response Measurement. The device was serially connected to a series resistor (50 Ω). A single square pulse (the rising and falling times were 300 ns, and the pulse width was 1 μs) was applied to the device TE. The voltage including the transient responses at the TE and BE were obtained from an oscilloscope (with both input resistances of CH1 and CH2 set to 1 MΩ). The net applied voltage and current in the device were $V_{DUT} = V_{CH1} - V_{CH2}$ and $I_{DUT} = V_{CH2}/50\ \Omega$, respectively.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Additional discussions about the detail of the forming step, the XPS data, activation energy for electrical transport (E_{AC}), detailed model derivation steps to extract the effective hopping distance (a), *ab initio* calculation procedure, and schematic of the V_O hopping processes. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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